Design AXI Master IP using Vivado HLS tool

Abstract

Vivado HLS (High-Level Synthesis) tool converts C, C++ and System C designs to RTL implementations which can be synthesized into a Xilinx FPGA. This application of the Vivado HLS tool facilitated easier and a faster methodology to design AXI Master block in “HEVC Decoder on Zynq”.

The AXI Master block is useful in transferring data from FPGA fabric to ARM-based Processor System and contributed significantly in improving the performance of the HEVC Decoder.

Introduction

FPGAs are very useful in realizing advanced applications in Wireless, Medical, Defense and Consumer applications. IPs based on advanced algorithms is the need for such applications. In such scenarios, Vivado High-Level Synthesis accelerates creation of IPs by enabling C, C++ or System C based specifications to be directly targeted to Xilinx All Programmable devices without the need of manually developing RTL (Register Transfer Logic) code.

Through Vivado HLS, the C, C++ or System C based specifications can be transformed into a RTL implementation that can be synthesized into Xilinx FPGA devices.

Vivado HLS thus bridges the Software and hardware domains. HLS allows Hardware engineers to take advantage of productivity benefits of working at a higher level of abstraction and create high performance hardware. For Software developers, HLS provides an easy way to accelerate the computationally intensive parts of algorithms on a new compiled target.

This paper details the usage of Vivado HLS in creating AXI-Master IP. The AXI-Master is an important component in implementing HEVC Decoder on Zynq.

The paper starts with a brief description of AXI Master and its advantages. Subsequent sections details the steps used in Vivado HLS to implement AXI master.
AXI Master

Managing Data traffic by ensuring correctness and fast transmission of data with memory devices is a critical task in Video-based designs. By definition, HEVC (H.265) standard achieves twice the data compression for the same video quality as compared to its predecessor H.264. Hence, implementation of HEVC Decoder necessitates fast and accurate data transfers.

The Xilinx Zynq FPGA is a new class of product that combines an industry-standard ARM® dual-core Cortex™ – A9 MPCore™ Processing System (PS) with Xilinx 28nm Programmable Logic (PL). This unique coalescing of technologies of PS and PL and powerful interconnects between them makes Zynq an ideal platform for Software-Hardware co-design. While Hardware provides better parallelism, Software takes care of Controlling Data traffic and processing of IPs.

Zynq uses AXI interconnect to facilitate data traffic between PS and PL. The PS portion has DDR memory that is mostly used in transferring and receiving huge chunks of data while transacting with the PL fabric. DMA (Direct Memory Access), Video DMA in particular, is used for such transfers of data. The Processing System (PS) controls the VDMA operation. A VDMA is triggered when the pertinent data is available in the DDR memory and needs to be transferred to the PL fabric for further computations.

The final decoded video will get its data from the frame buffer which sits in the PS controlled DDR. The computationally intensive blocks of the HEVC Decoder are implemented in the PL fabric. The final output data from the PL fabric should therefore be transferred back to the DDR memory.

There are 2 options to achieve transfer of data from the PL fabric to the DDR memory:

i. PL fabric sends a handshake signal to the PS indicating its readiness to transfer data. Upon receiving the handshake signal, the PS can trigger a VDMA operation and data can be received by the DDR from PL. Communication through handshake signals brings with it a significant consumption of Computational Cycles and this translates to a higher time required for data transfers. Besides, the VDMA, being PS controlled causes a drain on the bandwidth of ARM core.

ii. By using AX-Master, the final computed data can be directly transferred from the PL fabric to the DDR memory without any intervention of the ARM core. The need for handshake signal is avoided. And since the ARM processor is not involved, there is no drain on ARM bandwidth.
Data transfer from the PL fabric to the DDR memory controlled by AXI-Master fits in perfectly to ensure fast and accurate data transfers.

Design of AXI-Master can be done by RTL coding using Verilog or VHDL. With introduction of HLS in the Vivado Design suite, a simple C code can be developed to describe AXI master functionality. This significantly reduces the coding effort, both in complexity and time required.

The following section describes the methodology applied to design AXI-Master by the HLS tool.

**AXI-Master Design using HLS**

The HLS feature is integrated with the Vivado Design Suite and the license for the same is available with Vivado System Edition.

The tool is opened by clicking on the Vivado HLS icon.

A new project is created by:

- Entering Project name
- Include the Source ‘C’ file and Testbench
- Specify the Clock period for the design
- Identify the target board/part. In this project, the board is ZC706 and FPGA is Zynq 7045
The ‘C’ Source code describing the functionality of AXI Master is developed. HLS directive HLSINTERFACE is used to define AXI-Master port connections.

In this particular application, the AXI-Master does a 2D data transfer by taking the PL data and copying the same at the specified DDR location thro bursts. The width of data being transferred is 64 bits. Each burst involves 256 transactions. Hence a maximum of 256*8 = 2048 bytes can be transferred for each burst of AXI-Master. Since the transfer is a 2D type, the amount of data being transferred depends on hsize (Horizontal Size), vsize (Vertical Size) and Stride of the video frame.

The developed C code is synthesized and equivalent RTL code is generated in Verilog, VHDL and SystemC. Verilog Code is used in this project.

The resultant RTL code is the AXI-Master IP. This IP is packaged and exported to Vivado environment.
To use the AXI Master IP in the whole system, open the Vivado tool. Add the AXI Master into the IP Repositories and the same will be reflected in the IP Catalog.

This IP is now used in the Block Design of the HEVC Decoder. The master port of AXI Master is connected to slave port of Zynq PS thro AXI-HP interconnect.
Conclusion

The performance of the HEVC Decoder involving AXI Master for PL to PS communication improved by 50% when compared to performance of the HEVC Decoder involving AXI VDM S2MM Data transfer from PS to PL.

Hence, the impact of AXI Master in the design contributing to the increased performance is:

- Avoidance of handshakes between PL and PS based on which AXI VDMA (S2MM) was triggered from PS
- Reduced Bandwidth on ARM Core
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http://www.pathpartnertech.com/

sales@pathpartnertech.com