HEVC/H.265 Decoder on Zynq

Supported Features

- Main profile decoding up to level 5
- I, P, and B picture decoding
- Frame (Progressive) decoding
- All Coding Unit sizes (64x64 to 8x8)
- All Transform Unit sizes (32x32 to 4x4)
- All Intra prediction sizes and modes
- All Inter prediction unit sizes
- Asymmetric Motion Partitions (AMP)
- Weighted prediction
- Temporal Layers up to 4
- Quarter pixel motion compensation
- Slices
- In-loop Deblocking filter
- Sample Adaptive Offset filtering
- Constrained intra prediction
- PCM decoding
- Multi reference frames
- Video resolutions up to 1920x1080
- Multithreaded implementation
- Complaint to HM11.0 version
- Decoder data in YUV 4:2:0 planar format

Description

H.265 or MPEG-H Part 2 or High Efficiency Video Coding (HEVC) is the most contemporary video compression standard jointly developed by MPEG group of ISO/IEC and ITU-T. It is a successor to H.264 and expected to provide double the data compression ratio compared to H.264 at the same level of video quality. This HEVC Decoder is implemented on Zynq platform by utilizing Zynq’s architecture wherein Dual-core ARM Cortex-A9 based Processing System and Programmable Logic (Xilinx Artix 7) are integrated into a single device.

Target Performance:

1080p@30fps for 4Mbps bitstreams

FPGA implementation metrics:

The following is an estimate. Final numbers will be available after complete implementation

Xilinx Tool: ISE 14.2
Hardware Utilization

<table>
<thead>
<tr>
<th>LUT</th>
<th>BRAM</th>
<th>DSP Slices</th>
<th>Registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,00,000</td>
<td>140</td>
<td>150</td>
<td>60,000</td>
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**Frequency (Target):** 150 MHz

(The frequency presently achieved post Routing is 125 MHz, while individual blocks are functional at 200+ MHz post Synthesis)

![Diagram of HEVC Decoder on Xilinx Zynq FPGA](image)

**Acronyms:**

<table>
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<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>CABAC</td>
<td>Context Adaptive Binary Arithmetic Coding</td>
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<tr>
<td>SAO</td>
<td>Sample Adaptive Offset</td>
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<td>DPB</td>
<td>Decoder Picture Buffer</td>
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About PathPartner

PathPartner Technology based out of California, USA and Bangalore, India is a leading provider of products and services for multimedia centric embedded devices. PathPartner has extensive experience in audio & video codecs, video analytics & vision, imaging, multimedia middleware and application development.

PathPartner has an expert management team with rich experience in Technology, Engineering & Business practices. The company has Sales & marketing presence in USA, Europe, Korea, Taiwan and India. PathPartner specializes in addressing challenges faced by leading Silicon vendors, OS providers and OEMs in their product development.

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